FIG. 1

COMPRESSION / EXPANSION BUS

FRAME 1 MEMORY

MEMORY BUS

WRITING MEANS 3

SIGNAL REARRANGING MEANS 4

SUBSAMPLING AND READ-OUT MEANS (SKIPPING AT REGULAR INTERVALS) 5

HOST BUS

FRAME MEMORY CONTROLLER 2

VIDEO BUS

Fig. 2

TIME →

DATA TRANSFER CLOCK

(1) DCLK

(2) VBUS

VIDEO BUS

(3)

(4)

(2): R₀ G₀ B₀ R₁ G₁ B₁ R₂

(3): R₀ R₁ G₀ G₁ B₀ B₁ R₂

(4): R₀ R₁ R₂ G₀ G₁ G₂ B₀

FIG.3

	0	1	2	3	4	5
0	R_{00}	R_{01}	G_{00}	G_{01}	B_{00}	B_{01}
1	R_{10}	R_{11}	G_{10}	G_{11}	B_{10}	B_{11}
2	R_{20}	R_{21}	G_{20}	G_{21}	B_{20}	B_{21}
3	R_{30}	R_{31}	G_{30}	G_{31}	B_{30}	B_{31}

FIG. 4

COMPRESSION / EXPANSION BUS

Y BUS   MEMORY BUS   C BUS

FRAME
1. MEMORY

Y MEMORY
6

C MEMORY
7

WRITING MEANS
8

SUBSAMPLING AND READ-OUT MEANS
(SKIPPING AT REGULAR INTERVALS)
5

WRITING MEANS
3

SIGNAL REARRANGING
MEANS 4

VIDEO BUS

Y BUS   C BUS

FRAME MEMORY
2 CONTROLLER

HOST BUS

FIG. 5

HORIZONTAL ADDRESS

STORAGE ADDRESS OF C_B AND C_R SIGNAL (C MEMORY)

	0	1	2	3	4	5	6	7	
0	C_{B00}	C_{B02}	C_{R00}	C_{R02}	C_{B04}	C_{B06}	C_{R04}	C_{R06}	
1	C_{B10}	C_{B12}	C_{R10}	C_{R12}	C_{B14}	C_{B16}	C_{R14}	C_{R16}	
2	C_{B20}	C_{B22}	C_{R20}	C_{R22}	C_{B24}	C_{B26}	C_{R24}	C_{R26}	
3	C_{B30}	C_{B32}	C_{R30}	C_{R32}	C_{B34}	C_{B36}	C_{R34}	C_{R36}	

VERTICAL ADDRESS

FIG. 6

DATA TRANSFER CLOCK

Y SIGNAL (Y BUS)

C SIGNAL (C BUS)

TIME

FIG 7

STORAGE ADDRESS OF C_B AND C_R SIGNAL (C MEMORY)
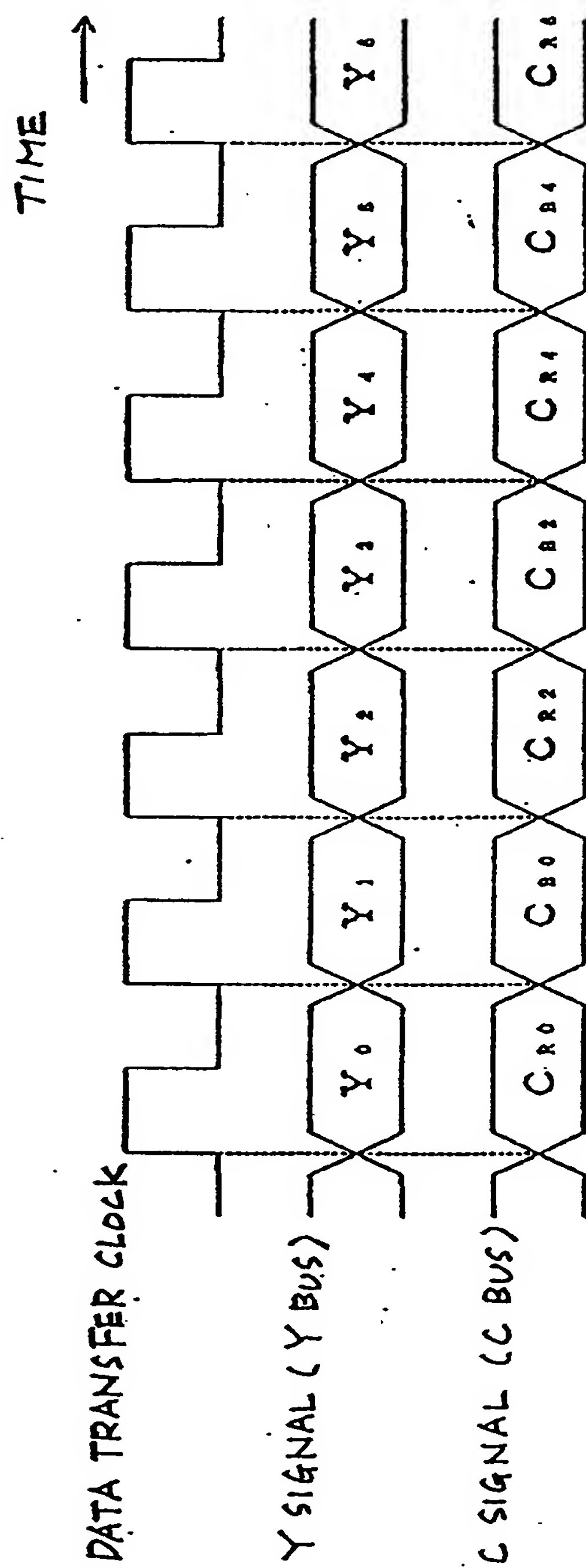
HORIZONTAL ADDRESS

	0	1	2	3	4	5	6	7
0	C_{R00}	C_{R01}	C_{B00}	C_{B02}	C_{R04}	C_{R05}	C_{B04}	C_{B06}
1	C_{R10}	C_{R11}	C_{B10}	C_{B11}	C_{R14}	C_{R15}	C_{B14}	C_{B16}
2	C_{R20}	C_{R21}	C_{B20}	C_{B21}	C_{R24}	C_{R25}	C_{B24}	C_{B26}
3	C_{R30}	C_{R31}	C_{B30}	C_{B31}	C_{R34}	C_{R35}	C_{B34}	C_{B36}

VERTICAL ADDRESS

FIG. 8

FIG. 9

FRAME MEMORY

1

MEMORY BUS

COMPRESSION / EXPANSION BUS

3

WRITING MEANS

8

READ-OUT MEANS

HOST BUS

VIDEO BUS

FRAME MEMORY CONTROLLER

2

FIG. 10

HORIZONTAL ADDRESS

INTERLACE SCANNING

HORIZONTAL ADDRESS

NON-INTERLACE SCANNING

VERTICAL ADDRESS
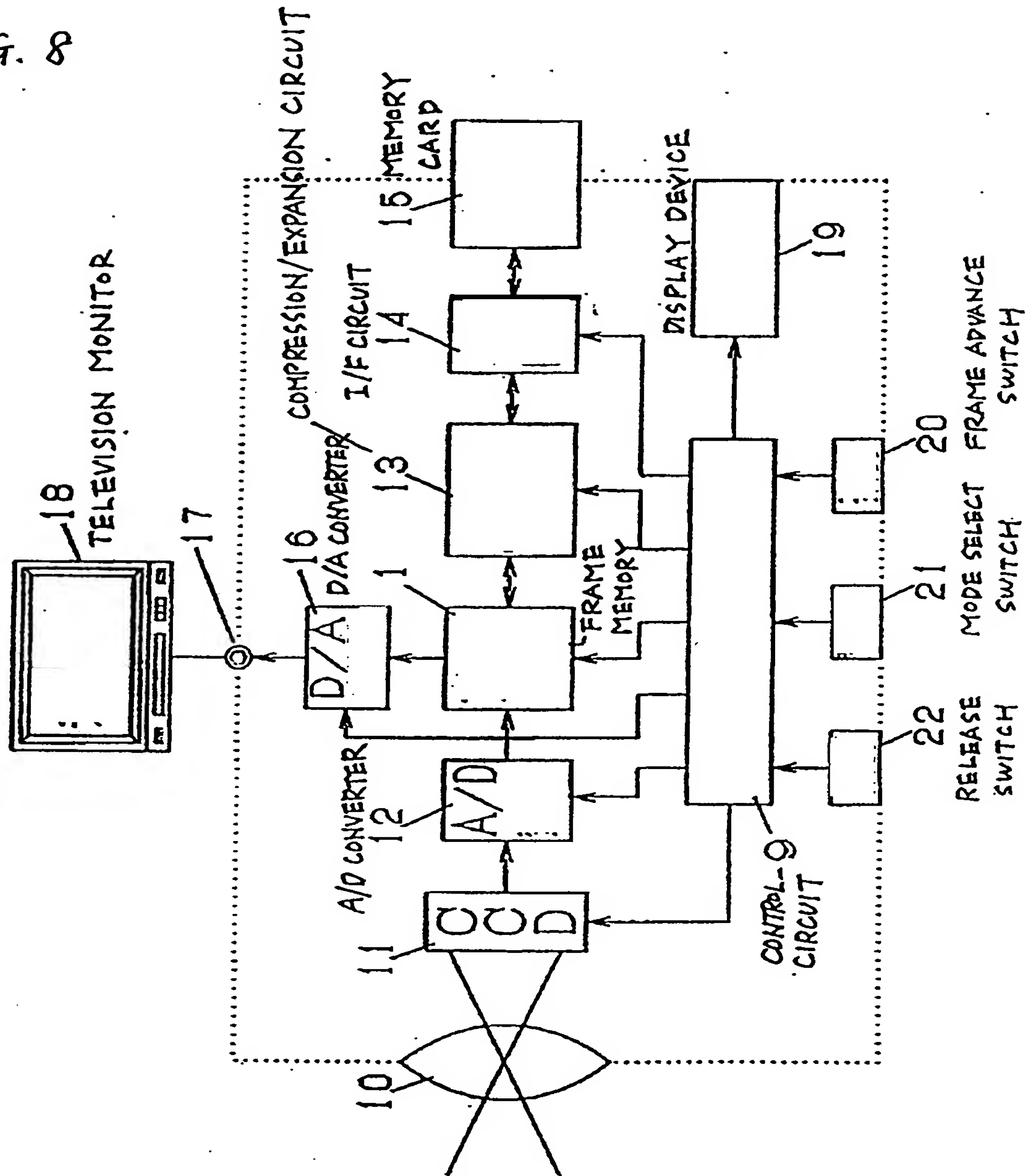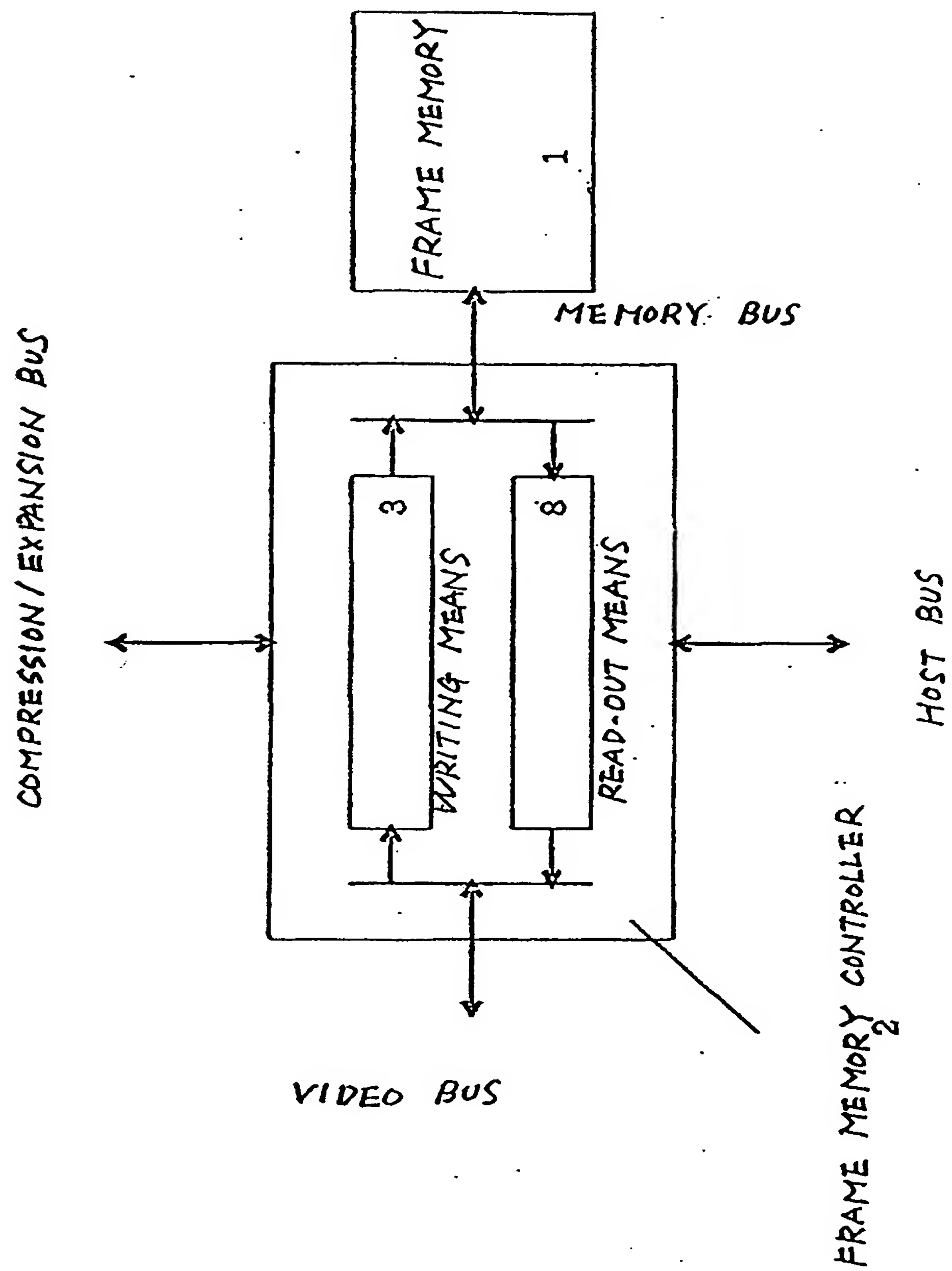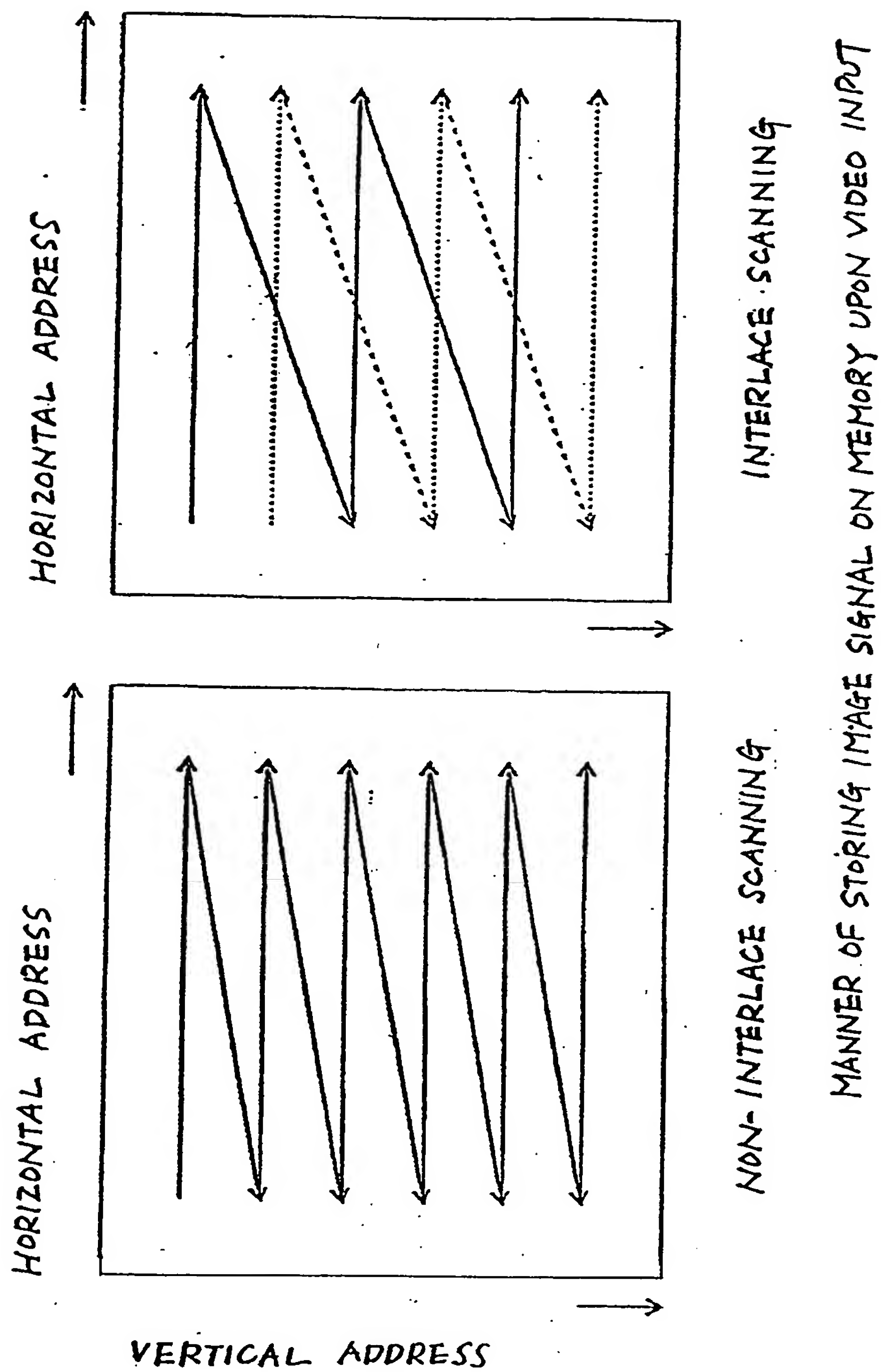
MANNER OF STORING IMAGE SIGNAL ON MEMORY UPON VIDEO INPUT

FIG. 11

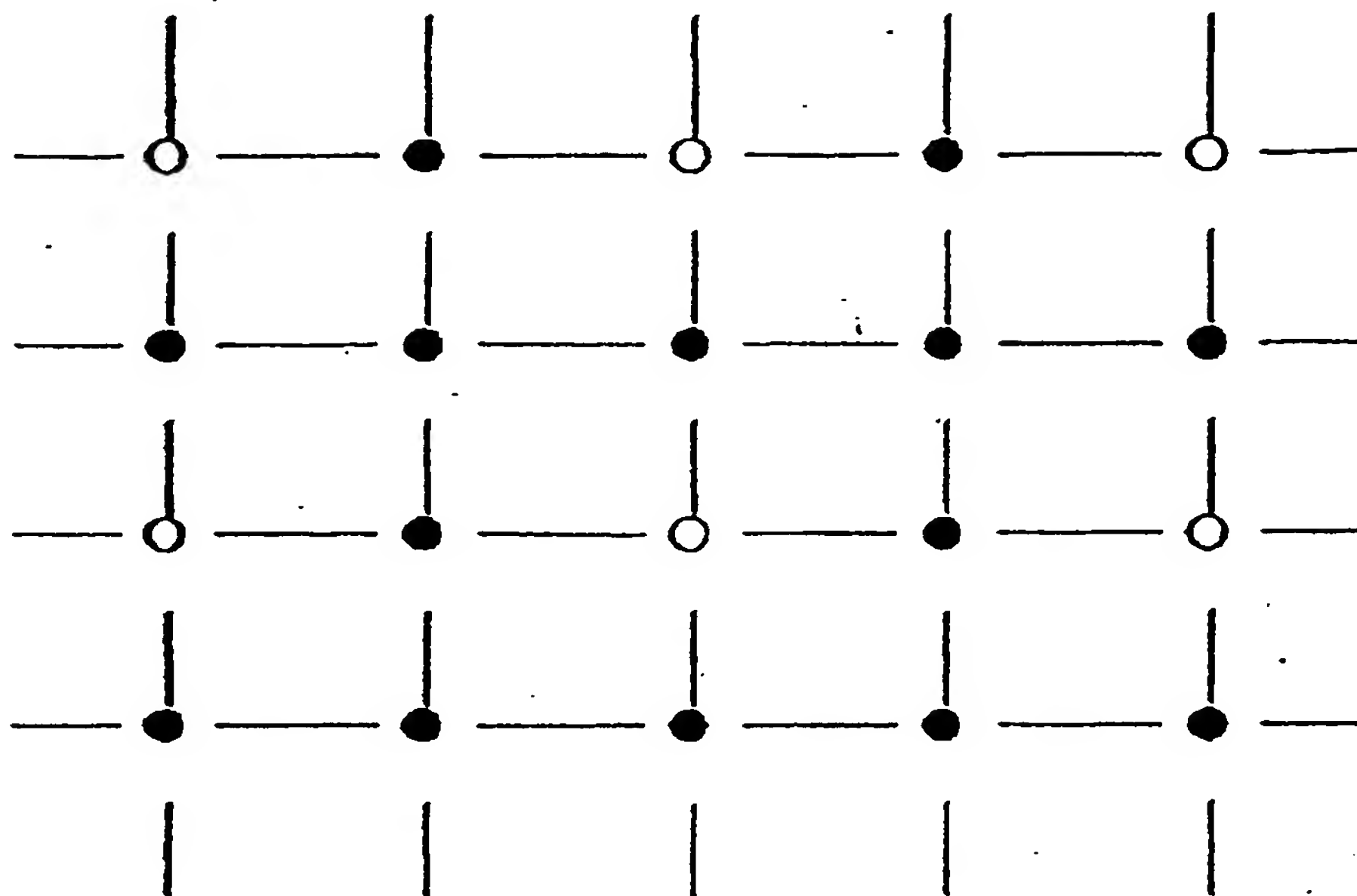| G	B	G	B	G	B	G	B	G
R	G	R	G	R	G	R	G	R
G	B	G	B	G	B	G	B	G
R	G	R	G	R	G	R	G	R
G	B	G	B	G	B	G	B	G
R	G	R	G	R	G	R	G	R
G	B	G	B	G	B	G	B	G
R	G	R	G	R	G	R	G	R

SINGLE DISC COLOR FILTER HAVING
BAYER ARRANGEMENT

FIG. 12
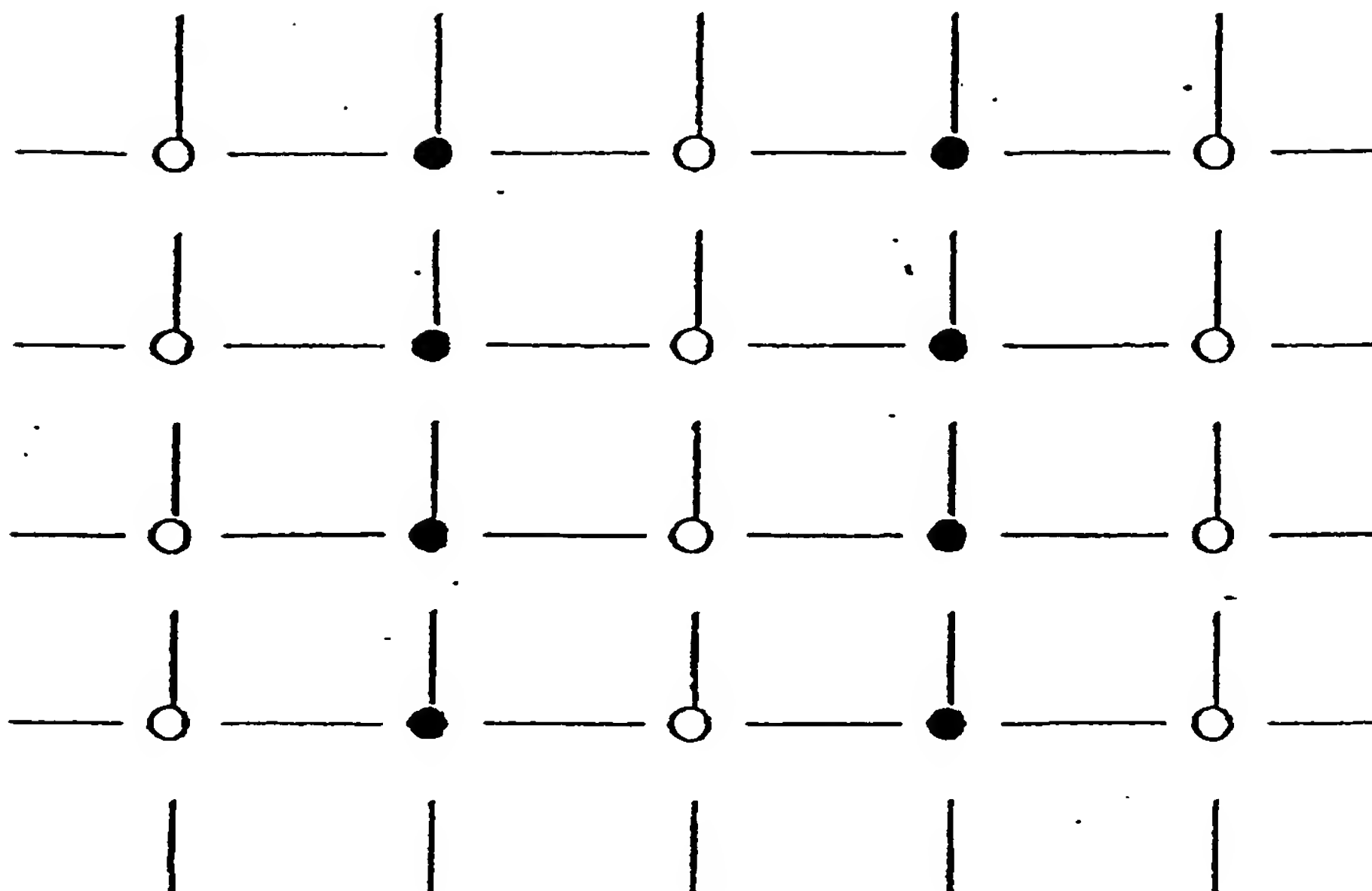
SAMPLING COORDINATES OF YC_BC_R 4:2:2
IMAGE SIGNAL

FIG. 13

SAMPLING COORDINATES OF YC_BC_R 4:1:1
IMAGE SIGNAL

FIG. 14

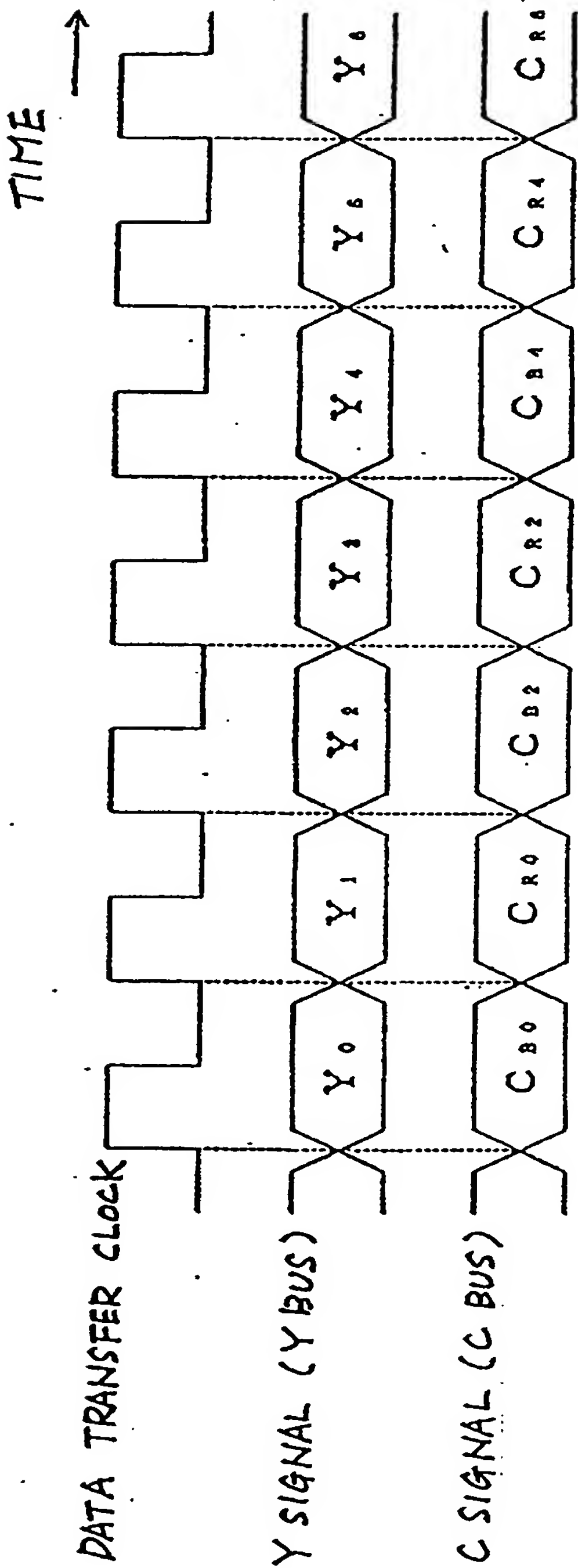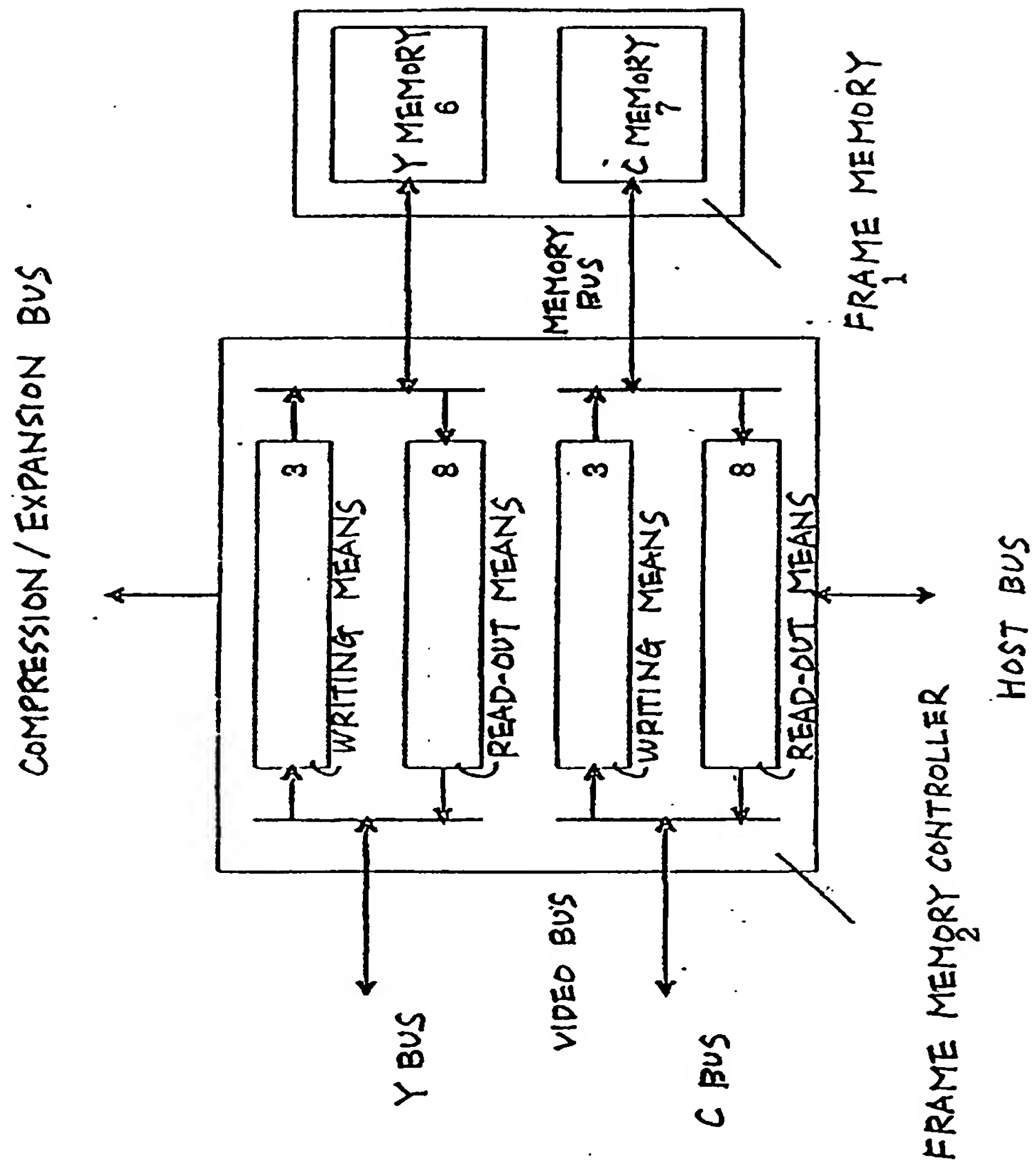

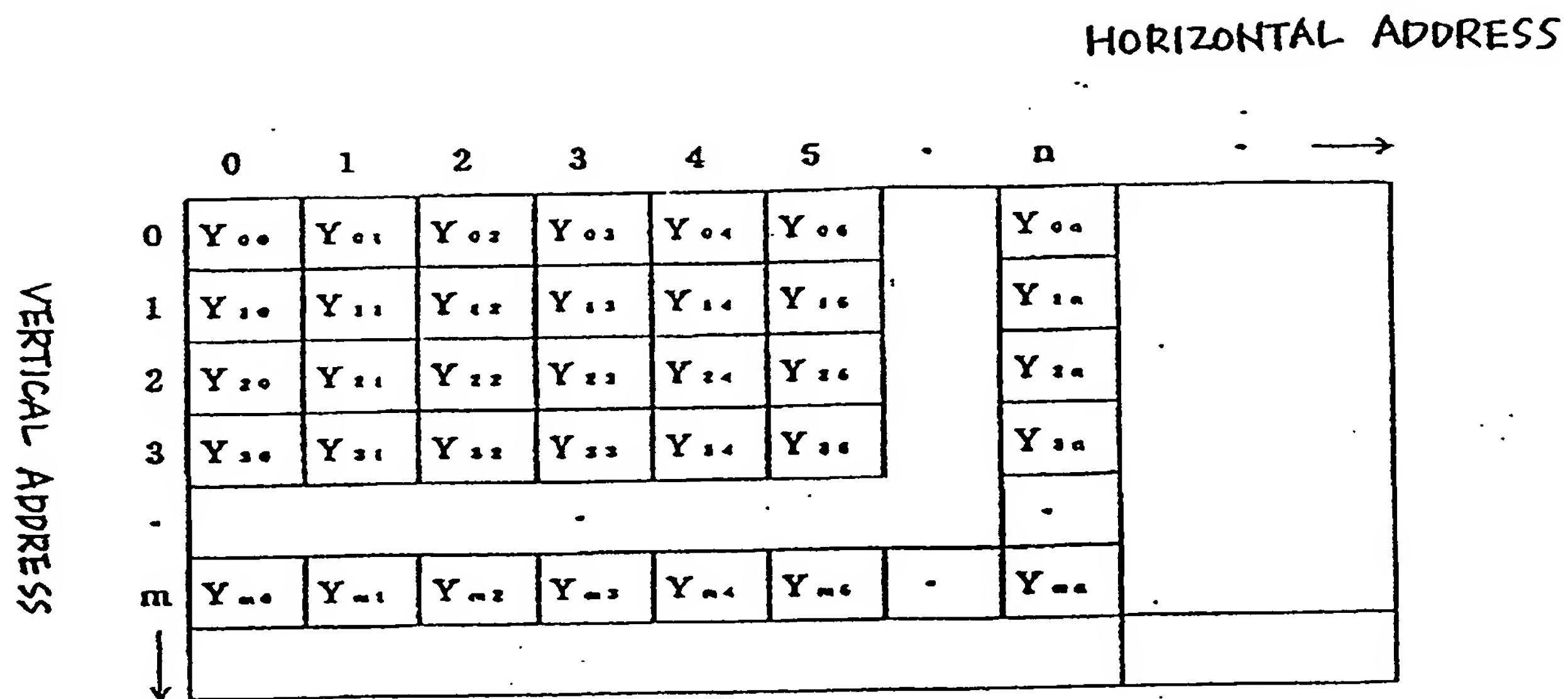TIME →

DATA TRANSFER CLOCK

Y SIGNAL (Y BUS) : Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6

C SIGNAL (C BUS) : C_{B0}, C_{R0}, C_{B2}, C_{R2}, C_{B4}, C_{R4}, C_{R6}

FIG. 15

COMPRESSION / EXPANSION BUS

Y MEMORY 6

C MEMORY 7

FRAME MEMORY 1

MEMORY BUS

WRITING MEANS 3

READ-OUT MEANS 8

WRITING MEANS 3

READ-OUT MEANS 8

Y BUS

VIDEO BUS

C BUS

FRAME MEMORY CONTROLLER 2

HOST BUS

FIG. 16 (a)

HORIZONTAL ADDRESS

STORAGE ADDRESS OF Y SIGNAL (Y MEMORY)

FIG. 16 (b)

HORIZONTAL ADDRESS
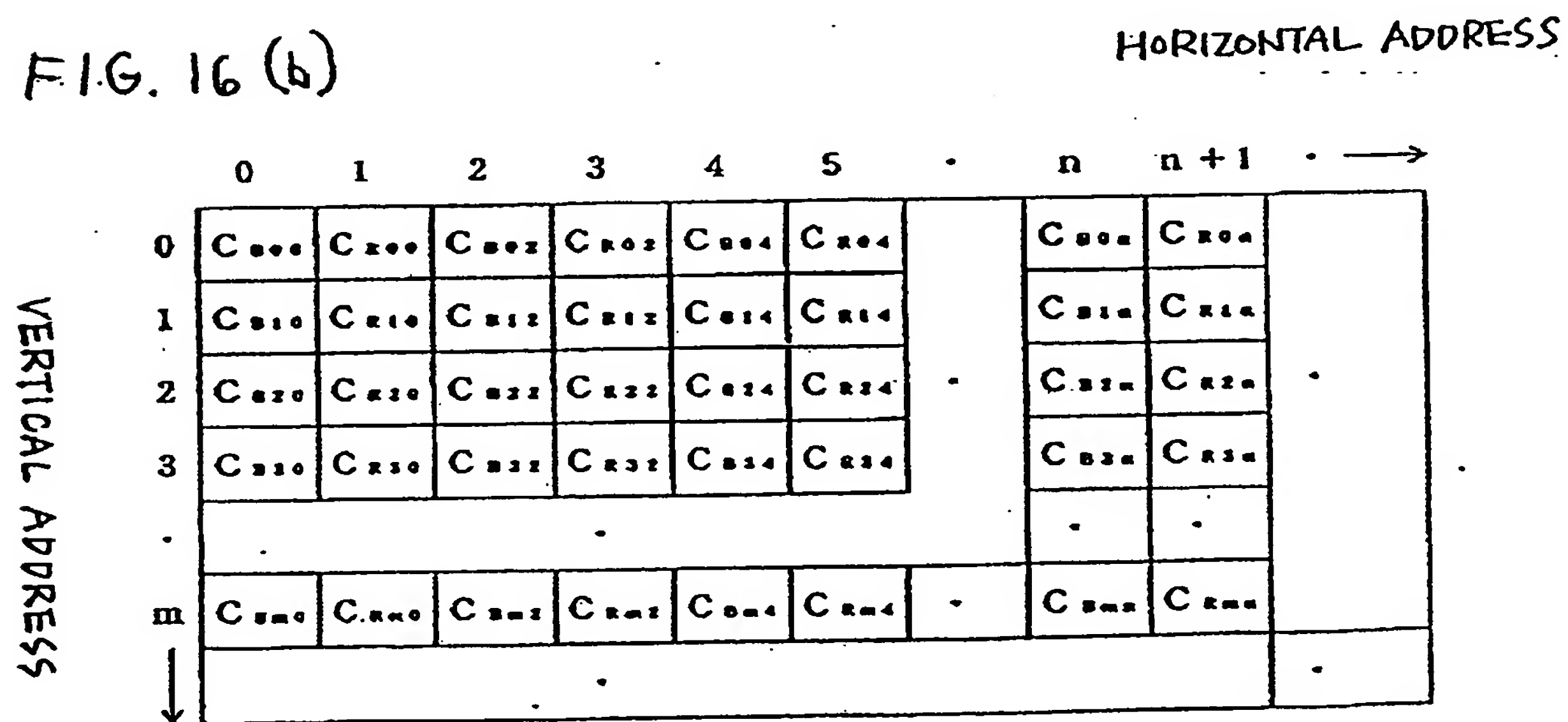
IN THIS CASE, n IS INTEGER

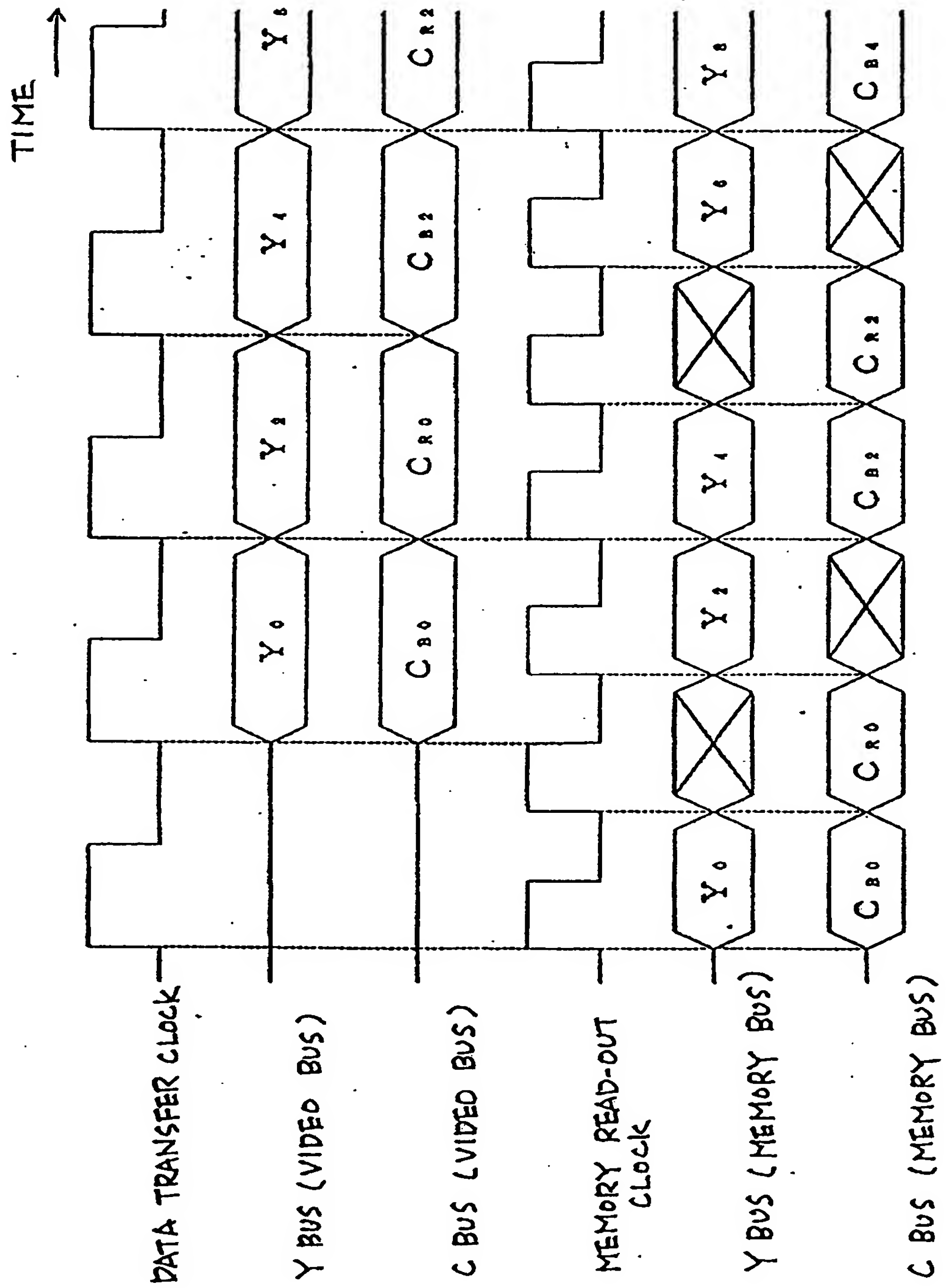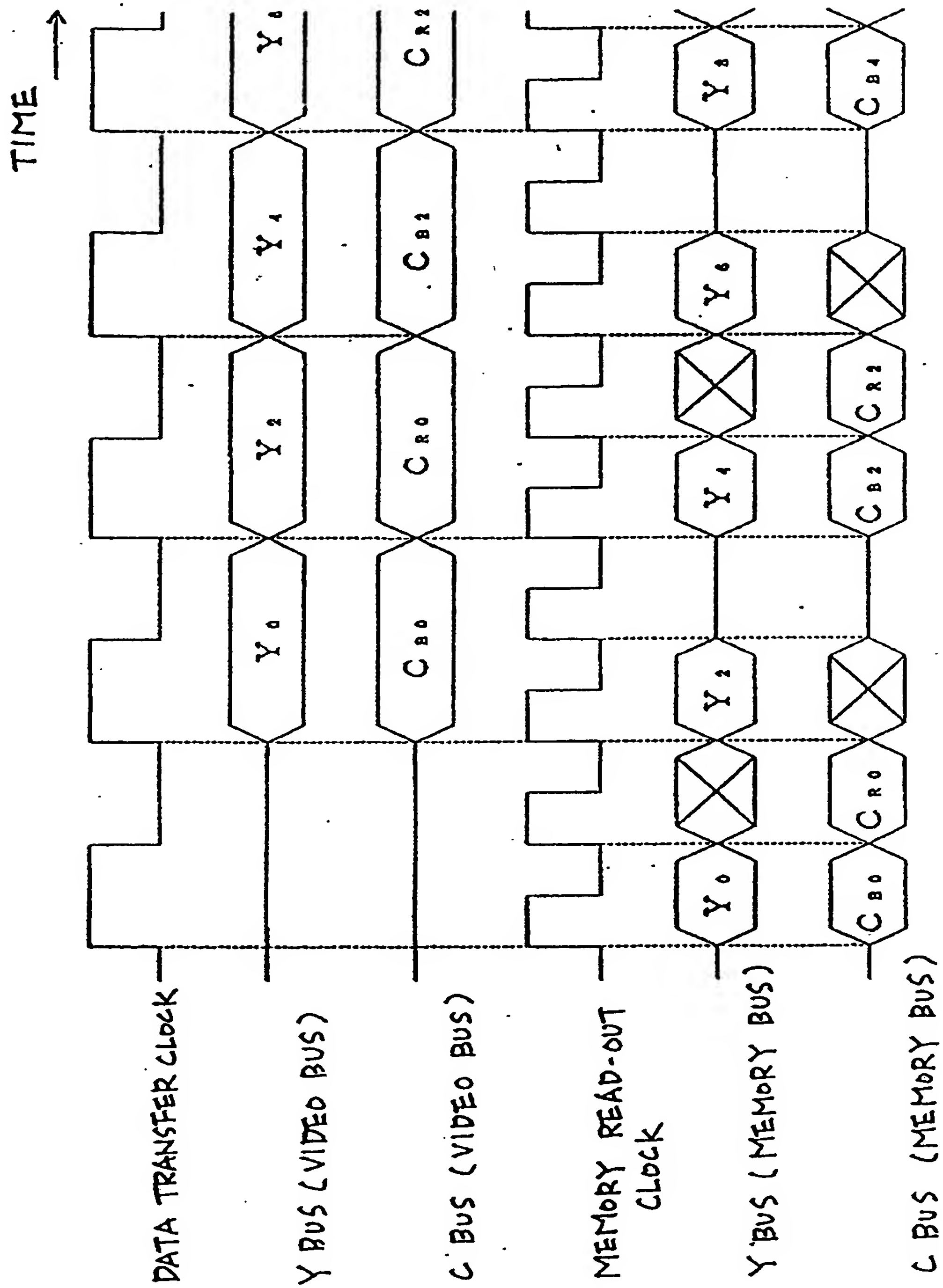STORAGE ADDRESS OF C_B AND C_R SIGNAL (C MEMORY)

FIG. 17

TIME

DATA TRANSFER CLOCK

Y BUS (VIDEO BUS)

C BUS (VIDEO BUS)

MEMORY READ-OUT CLOCK

Y BUS (MEMORY BUS)

C BUS (MEMORY BUS)

FIG. 18

TIME →

DATA TRANSFER CLOCK

Y BUS (VIDEO BUS)

C BUS (VIDEO BUS)

MEMORY READ-OUT CLOCK

Y BUS (MEMORY BUS)

C BUS (MEMORY BUS)

Fig. 19